NJD1718, NJVNJD1718

Power Transistors

PNP Silicon DPAK For Surface Mount Applications

Designed for high−gain audio amplifier and power switching applications.

Features

- Low Collector−Emitter Saturation Voltage
- High Switching Speed
- Epoxy Meets UL 94 V−0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Base Voltage	V_{CB}	−50	Vdc
Collector−Emitter Voltage	V_{CEO}	−50	Vdc
Emitter−Base Voltage	V_{EB}	−5	Vdc
Collector Current − Continuous	I_C	−2	Adc
Collector Current − Peak	I_{CM}	−3	Adc
Base Current	I_B	−0.4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 15 0.1	 W W/°C
Total Device Dissipation @ T_A = 25°C (Note 1) Derate above 25°C	P_D	 1.68 0.011	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C
ESD − Human Body Model	HBM	3B	V
ESD − Machine Model	MM	C	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

THERMAL CHARACTERISTICS

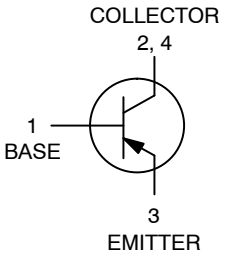
Characteristic	Symbol	Max	Unit
Thermal Resistance Junction−to−Case Junction−to−Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$	 10 89.3	°C/W

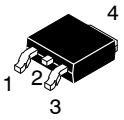
2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ON Semiconductor®

http://onsemi.com

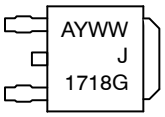
SILICON
POWER TRANSISTORS
2 AMPERES
50 VOLTS
15 WATTS





DPAK
CASE 369C
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NJD1718T4G	DPAK (Pb−Free)	2500 / Tape & Reel
NJVNJD1718T4G	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (Note 3) (I_C = −10 mAdc, I_B = 0)	BV_{CEO}	−50		–	Vdc
Collector Cutoff Current (V_{CB} = −50 Vdc, I_E = 0)	I_{CBO}	–		−100	nAdc
Emitter Cutoff Current (V_{BE} = −5 Vdc, I_C = 0)	I_{EBO}	–		−100	nAdc
ON CHARACTERISTICS					
DC Current Gain (Note 3) (I_C = −0.5 A, V_{CE} = 2 V) (I_C = −1.5 Adc, V_{CE} = 2 Vdc)	h_{FE}	70 40		240 –	–
Collector−Emitter Saturation Voltage (Note 3) (I_C = −1 A, I_B = −0.05 A)	$V_{CE(sat)}$	–	−0.2	−0.5	Vdc
Base−Emitter Saturation Voltage (Note 3) (I_C = −1 A, I_B = −0.05 Adc)	$V_{BE(sat)}$	–	–	−1.2	Vdc
Base−Emitter On Voltage (Note 3) (I_C = −1 Adc, V_{CE} = −2 Vdc)	$V_{BE(on)}$	–	–	−1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (Note 4) (I_C = −500 mAdc, V_{CE} = −2 Vdc, f_{test} = 10 MHz)	f_T	–	80	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	33	–	pF
Switching Timers V_{CC} = −30 V, I_C = −1 A	t_{ON}	–	55	–	ns
	t_{STG}	–	320	–	
	t_f	–	40	–	

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
4. $f_T = |h_{fe}| \bullet f_{test}$.

TYPICAL CHARACTERISTICS

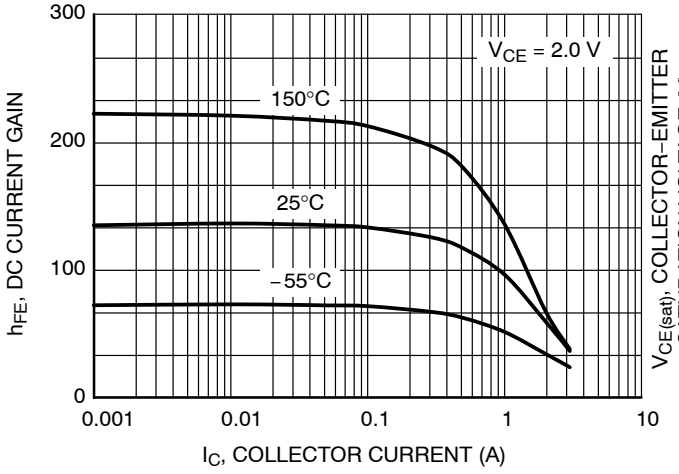


Figure 1. DC Current Gain

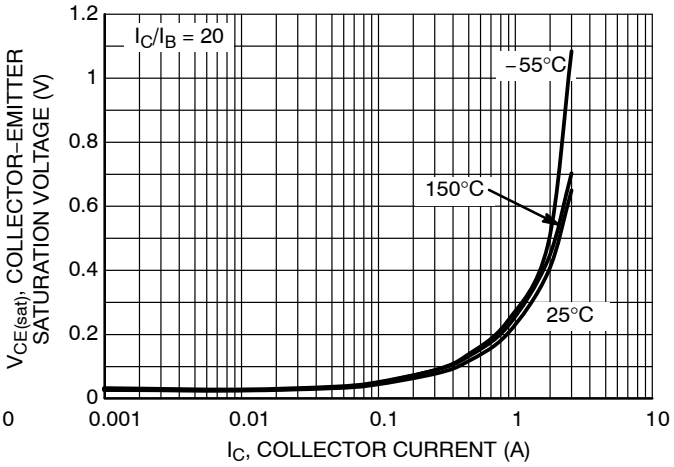


Figure 2. Collector−Emitter Saturation Voltage

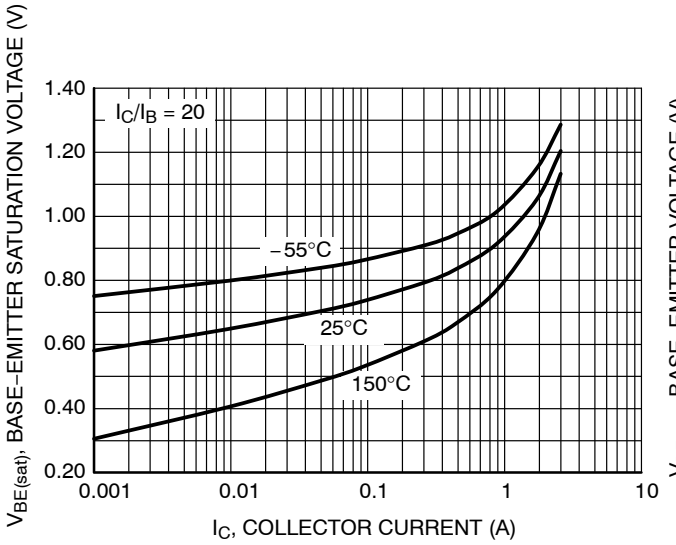


Figure 3. Base−Emitter Saturation Voltage

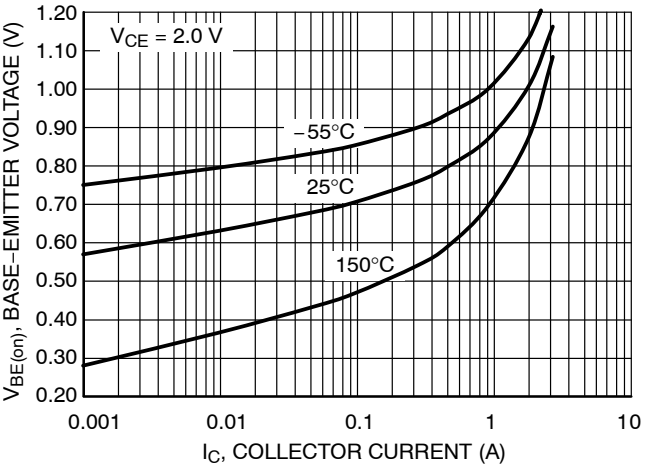


Figure 4. Base−Emitter Voltage

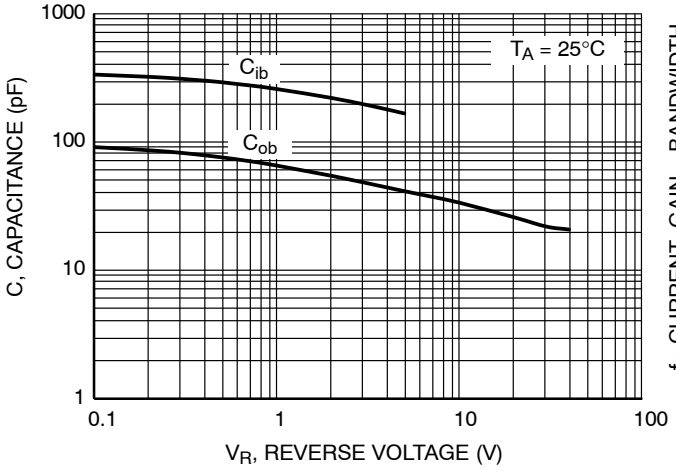


Figure 5. Capacitance

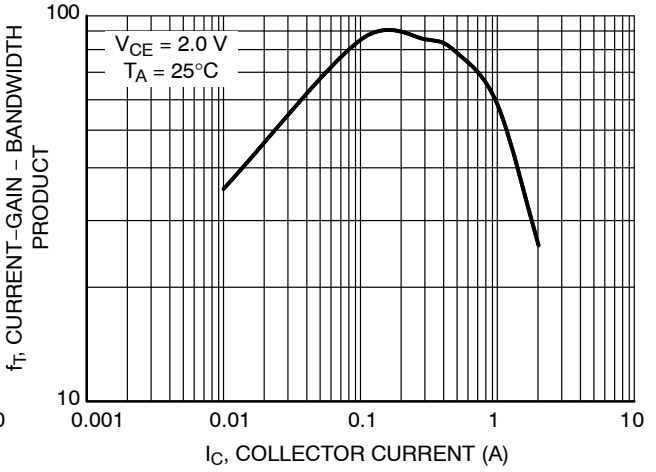


Figure 6. Current−Gain−Bandwidth Product

TYPICAL CHARACTERISTICS

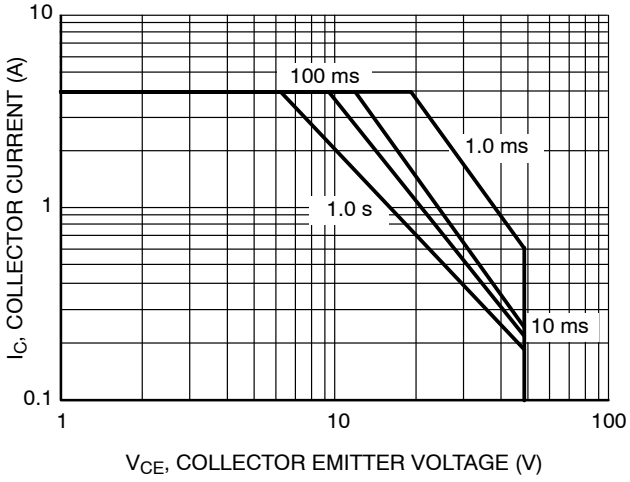


Figure 7. State Operating Area

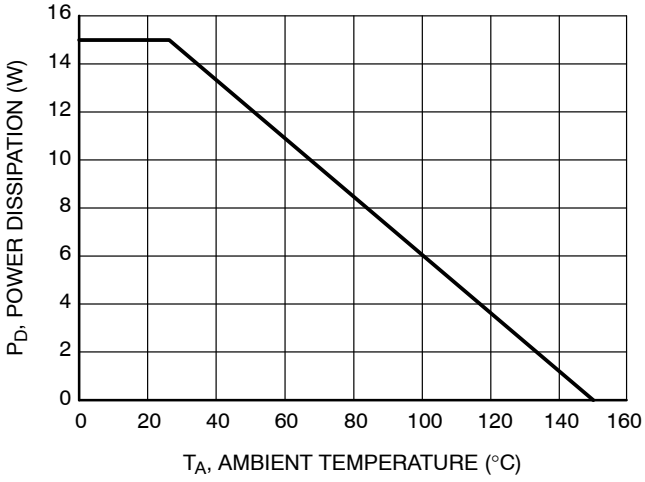


Figure 8. Power Derating

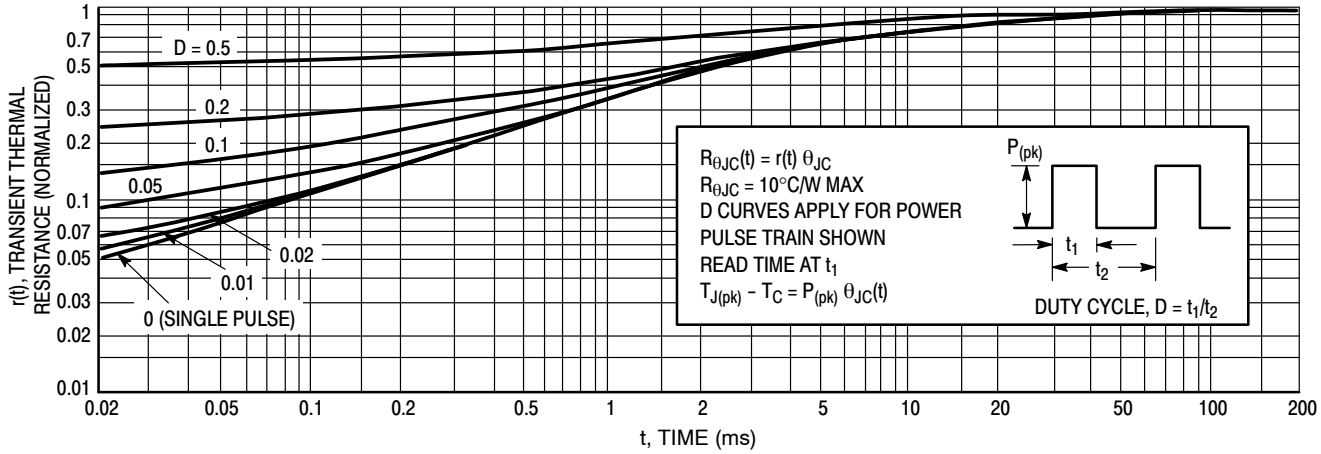
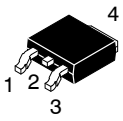


Figure 9. Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

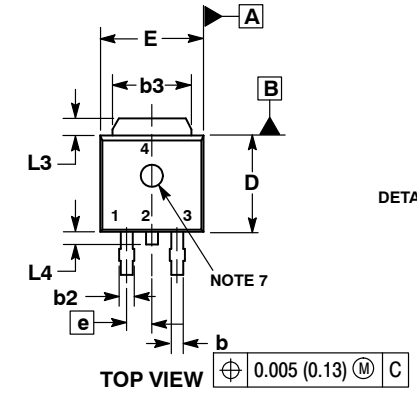
ON Semiconductor®

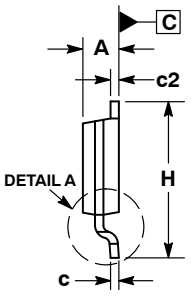


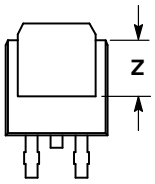
SCALE 1:1

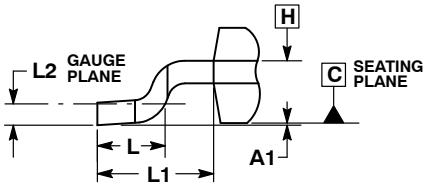
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

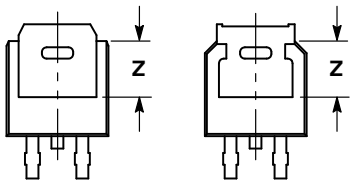
DATE 21 JUL 2015











NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

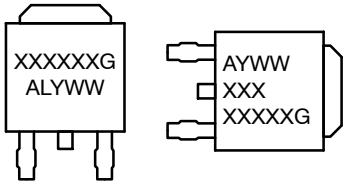
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

GENERIC MARKING DIAGRAM*

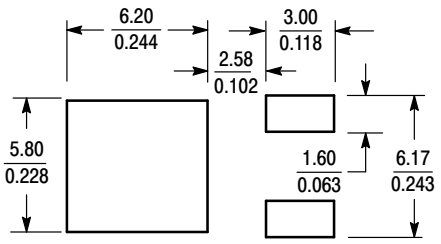


IC Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊